Complete 16-Channel, 12-Bit Data Acquisition Systems

AD363/AD364

FEATURES

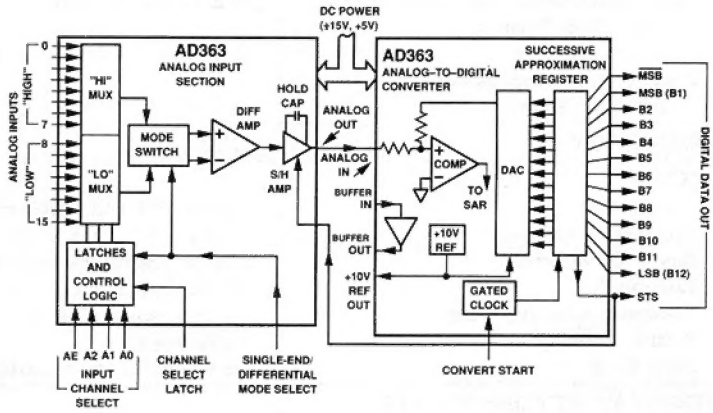
AD363

16-Channel Data Acquisition Input Stage with:
- Digitally Controlled Channel Selection/Mode Control
- 16 Single-Ended or 8 Differential Channels
- 25 kHz Throughput Rate
- Guaranteed No Missing Codes Over Temperature

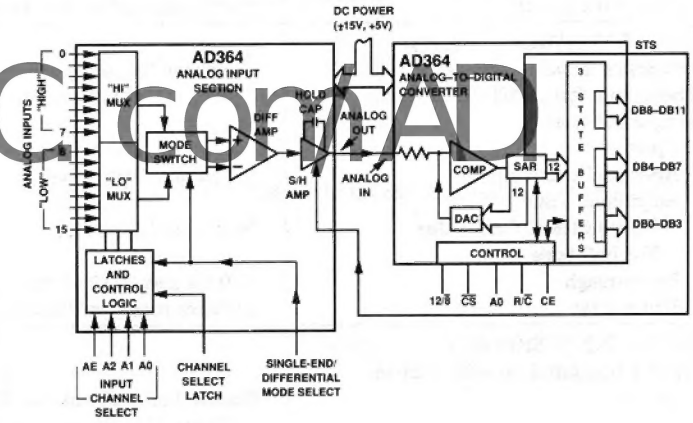
AD364

16-Channel Data Acquisition Input Stage with:
- Digitally Controlled Channel Selection/Mode Control
- 16 Single-Ended or 8 Differential Channels
- 20 kHz Throughput Rate
- Guaranteed No Missing Codes Over Temperature
- Three-State Buffered Digital Output

AD363 FUNCTIONAL BLOCK DIAGRAM



AD364 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTIONS

The AD363 and AD364 are complete 16-channel data acquisition systems which condition and subsequently convert an analog voltage into digital form. Each system consists of two devices, an analog input stage (AIS) and an analog-to-digital converter (ADC). The AIS includes a two 8-channel multiplexers, a channel address register, a unity gain instrumentation amplifier, and a sample-hold amplifier. The multiplexers may be connected to the instrumentation amplifier in either an 8-channel differential or 16-channel single ended configuration. A unique feature of these products is an internal user controlled switch which connects the multiplexers in either single-ended or differential mode. This allows a single device to perform in either mode with hard-wire programming and permits interfacing a mixture of single-ended and differential signals by dynamically switching the input mode control.

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The AD363 and AD364 differ in ADC performance. Each ADC is a complete 12-bit successive approximation converter including an internal clock and a precision reference. Active laser trimming results in maximum linearity errors of ±0.012% with conversion times of 25 μs (AD363) or 32 μs (AD364). The hybrid AD363-ADC has five user selectable input ranges (±2.5, ±5.0, ±10.0, 0 to +5, and 0 to +10 volts) and includes a high impedance buffer amplifier. The AD364-ADC is a monolithic converter with 3-state output buffer circuitry for direct interface to an 8-, 12-, or 16-bit processor bus and three user selected input ranges (±5, ±10, and 0 to +10 volts).

Both products are specified for operation over both the commercial (0°C to +70°C) and military (−55°C to +125°C) temperature ranges. The AD363 and AD364 are available with environmental screening. Please contact the factory or nearest sales office for details.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

AD363/AD364 – SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Parameter	AD363RK	AD363RS
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5 V, ±5.0 V, ±10.0 V	*
Unipolar	0 to +5 V, 0 to +10 V	*
Input (Bias) Current, per Channel	±50 nA max	*
Input Impedance		
ON Channel	10^{10} Ω, 100 pF	*
OFF Channel	10^{10} Ω, 10 pF	*
Input Fault Current (Power OFF or ON)	20 mA, max, Internally Limited	*
Common-Mode Rejection		
Differential Mode	70 dB min (80 dB) typ) @ 1 kHz, 20 V p–p	*
Mux Crosstalk (Interchannel,		
Any OFF Channel to Any ON Channel)	−80 dB max (−90 dB typ) @ 1 kHz, 20 V p–p	*
RESOLUTION	12 Bits	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adjustable to Zero)	*
Unipolar Offset Error	±10 mV (Adjustable to Zero)	*
Bipolar Offset Error	±20 mV (Adjustable to Zero)	*
Linearity Error	±1/2 LSB max	*
Differential Linearity Error	±1 LSB max (±1/2 LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1 mV p–p, 0.1 Hz to 1 MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30 ppm/°C max (±10 ppm/°C typ)	±25 ppm/°C max (±15 ppm/°C typ)
Offset, ±10 V Range	±15 ppm/°C max (±5 ppm/°C typ)	±8 ppm/°C max (±5 ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25 µs max (22 µs typ)	*
Throughput Rate, Full Rated Accuracy	25 kHz min (30 kHz typ)	*
Sample-and-Hold		
Aperture Delay	200 ns max (150 ns typ)	*
Aperture Uncertainty	500 ps max (100 ps typ)	*
Acquisition Time		
To ±0.01% of Final Value	18 µs max (10 µs typ)	*
For Full-Scale Step		
Feedthrough	−70 dB max (−80 dB typ) @ 1 kHz	*
Droop Rate	2 mV/ms max (1 mV/ms typ)	*
DIGITAL INPUT SIGNALS[3]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200 ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion	*
	1 TTL Load	*
Input Channel Select (to Analog Input Section, Pins 28–31)	4-Bit Binary Channel Address	*
	1 LS TTL Load	*
Channel Select Latch (to Analog (Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4 LS TTL Loads	*
Sample-Hold Command (to Analog Input Section Pin 13 Normally Connected to ADC "Status," Pin 20)	"0" Sample Mode	*
	"1" Hold Mode	*
	2 LS TTL Loads	*
Short Cycle (to ADC Section Pin 14)	Connect to +5 V for 12-Bits Resolution Connect to Output Bit n + 1 for n Bits Resolution	*
	1 TTL Load	*
Single-Ended/Differential Mode Select (to Analog Input Section, Pin 1)	"0" Single Ended Mode	*
	"1" Differential Mode (+4.0 V min)	*
	3 TTL Loads	*

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Parameter	AD363RK	AD363RS
DIGITAL OUTPUT SIGNALS[3]		
(All Codes Positive True)		
Parallel Date		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Twos Complement	*
Output Drive	2 TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2 TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2 TTL Loads	*
Internal Clock		
Output Drive	2 TTL Loads	*
Frequency	500 kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00 V, ±10 mV	*
Max External Current	±1 mA	*
Voltage Temperature Coefficient	±20 ppm/°C max	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15 V, ±5% @ +45 mA max (+38 mA typ)	*
	−15 V, ±5% @ −45 mA max (−38 mA typ)	*
	+5 V, ±5% @ +136 mA max (+113 mA typ)	*
Total Power Dissipation	2 Watts max (1.7 Watts typ)	*
TEMPERATURE RANGE		
Specification	0°C to +70°C	−55°C to +125°C
Storage	−55°C to +150°C	−55°C to +150°C
PACKAGE OPTIONS		
Analog Input Section (DH-32E)	AD363RKD	AD363RSD
AD Section (DH-32C)	AD363RKD	AD363RSD

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NOTES
[1]With 50 Ω, 1% fixed resistor in place of Gain Adjust pot.
[2]Conversion time of ADC Section.
[3]One TTL Load is defined as I_{IL} = −1.6 mA max @ V_{IL} = 0.4 V, I_{IH} = 40 μA max @ V_{IH} = 2.4 V. One LS TTL Load is defined as I_{IL} = −0.36 mA max @ V_{IL} = 0.4 V, I_{IH} = 20 μA max @ V_{IH} = 2.7 V.
*Specifications same as AD363RK.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply . . . . . +5.5 V
+V, Analog Supply . . . . . +16 V
−V, Analog Supply . . . . . −16 V
V_{IN}, Signal . . . . . ±V, Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1 V

AD363 PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION

Pin Number	Function
1	Single-End/Differential Mode Select
	"0": Single-Ended Mode
	"1": Differential Mode (+4.0 V min)
2	Digital Ground
3	Positive Digital Power Supply, +5 V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	No Connect
13	Sample-Hold Command
	"0": Sample Mode
	"1": Hold Mode
	Normally Connected to ADC Pin 20
14	Offset Adjust
15	Offset Adjust
16	Analog Output
	Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, −15 V
21	Positive Analog Power Supply, +15 V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch
	"0": Latched
	"1": Latch "Transparent"

ANALOG-TO-DIGITAL CONVERTER SECTION

Pin Number	Function
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1}}$ ($\overline{\text{MSB}}$) Out
14	Short Cycle Control
	Connect to +5 V for 12 Bits
	Connect to Bit (n + 1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5 V
17	$\overline{\text{Status}}$ Out
	"0": Conversion in Progress (Parallel Data Not Valid)
	"1": Conversion Complete (Parallel Data Valid)
18	+10 V Reference Out
19	Clock Out (Runs During Conversion)
20	Status Out
	"0": Conversion Complete (Parallel Data Valid)
	"1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In
	Reset Logic
	Start Convert
22	Comparator In
23	Bipolar Offset
	Open for Unipolar Inputs
	Connect to ADC Pin 22 for Bipolar Inputs
24	10 V Span R In
25	20 V Span R In
26	Analog Ground
27	Gain Adjust
28	Positive Analog Power Supply, +15 V
29	Buffer Out (for External Use)
30	Buffer In (for External Use)
31	Negative Analog Power Supply, −15 V
32	Serial Data Out
	Each Bit Valid on Trailing
	Edge Clock Out, ADC Pin 19

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SPECIFICATIONS (typical @ +25°C, ±15 V and +5 V unless otherwise noted)

Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA
Input Impedance ON Channel	10^{10}‖100	*	*	*	Ω‖pF
OFF Channel	10^{10}‖10	*	*	*	Ω‖pF
Input Fault Current	20	*	*	*	mA max
(Power ON or OFF)					(Internally
Common-Mode Rejection					Limited)
Differential Mode 1 kHz 20 V p–p	70 min (80 typ)	*	*	*	dB
Mux Crosstalk (Any OFF CHANNEL to Any ON Channel) 1 kHz 20 V p–p	−80 max (−90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1 mV p–p 0.1 Hz to 1 MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10 V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0°C to +70°C	*	−55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	µs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample-Hold					
Aperture Delay	200 max (150 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full-Scale Step	18 max (10 typ)	*	*	*	µs
Feedthrough at 1 kHz	−70 max (−80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single-Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential (+4 V min)	*	*	*	
	3 TTL Loads	*	*	*	
Sample-and-Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1 TTL Load	*	*	*	
ADC Section[3] $4.5 \leq V_L \leq 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	20	*	*	*	µA max
Logic "0"	20	*	*	*	µA max

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Parameter	AD364RJ	AD364RK	AD364RS	AD364RT	Units
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4 V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4 V	0.5	*	*	*	mA min
Output Leakage When in Three State	±40	*	*	*	μA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15 V, ±5% @ 36 mA max	*	*	*	
	−15 V, ±5% @ 65 mA max	*	*	*	
	+5 V, ±5% @ 75 mA max	*	*	*	
PACKAGE OPTIONS					
Analog Input Section (DH-32E)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	
ADC Section (D-28)	AD364RJD	AD364RKD	AD364RSD	AD364RTD	

NOTES
[1]With 50 Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2]Adjustable to zero.
[3]12/8 line must be hard wired to V_{LOGIC} or digital common.

*Specifications same as AD364RJ.
**Specifications same as AD364RK
***Specifications same as AD364RS.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply . . . . . +5.5 V
+V, Analog Supply . . . . . +16 V
−V, Analog Supply . . . . . −16 V
V_{IN}, Signal . . . . . ±V, Analog Supply
V_{IN}, Digital . . . . . 0 to +V, Digital Supply
AGND to DGND . . . . . ±1 V

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AD364 PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION		ANALOG-TO-DIGITAL CONVERTER SECTION	
Pin Number	**Function**	**Pin Number**	**Function**
1	Single-End/Differential Mode Select "0" Single-Ended Mode "1" Differential Mode	1	Logic Power Supply, +5 V
2	Digital Common	2	Data Mode Select (12/$\overline{8}$) "0": 8 Upper Bits or 4 Lower Bits as Selected by Byte Select (A_0))
3	Positive Digital Power Supply, +5 V	3	Chip Select ($\overline{CS}$) "0": Device Selected "1": Device Inhibited
4	"High" Analog Input, Channel 7	4	Byte Address/Short Cycle (A_0) "0": Upper 8 Bits Enabled (12/$\overline{8}$ "0")/ 12-Bit Cycle "1": Lower 4 Bits Enabled (12/$\overline{8}$ "1")/ 8-Bit Cycle
5	"High" Analog Input, Channel 6	5	Read Convert (R/$\overline{C}$) "0": Convert Start "1": Read Enable
6	"High" Analog Input, Channel 5	6	Chip Enable (CE) ↓ : R/$\overline{C}$ "0," $\overline{CS}$ "0" Initiates Conversion ↓ : R/$\overline{C}$ "1," $\overline{CS}$ "0" Initiates Read "0": Device Disabled "1": Device Enabled
7	"High" Analog Input, Channel 4	7	Analog Power Supply, +15 V (V_{CC})
8	"High" Analog Input, Channel 3	8	Reference Out, +10 V
9	"High" Analog Input, Channel 2	9	Analog Common (AC)
10	"High" Analog Input, Channel 1	10	Reference In
11	"High" Analog Input, Channel 0	11	Analog Power Supply, −15 V (V_{EE})
12	No Connect	12	Bipolar Offset
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 28	13	10 V Span Input
14	Offset Adjust	14	20 V Span Input
15	Offset Adjust	15	Digital Common (DC)
16	Analog Output Normally Connected to ADC "Analog In"	16	Data Bit 0
17	Analog Common	17	Data Bit 1
18	"High" ("Low") Analog Input, Channel 15 (7)	18	Data Bit 2
19	"High" ("Low") Analog Input, Channel 14 (6)	19	Data Bit 3
20	Negative Analog Power Supply, −15 V	20	Data Bit 4
21	Positive Analog Power Supply, +15 V	21	Data Bit 5
22	"High" ("Low") Analog Input, Channel 13 (5)	22	Data Bit 6
23	"High" ("Low") Analog Input, Channel 12 (4)	23	Data Bit 7
24	"High" ("Low") Analog Input, Channel 11 (3)	24	Data Bit 8
25	"High" ("Low") Analog Input, Channel 10 (2)	25	Data Bit 9
26	"High" ("Low") Analog Input, Channel 9 (1)	26	Data Bit 10
27	"High" ("Low") Analog Input, Channel 8 (0)	27	Data Bit 11
28	Input Channel Select, Address Bit AE	28	Status Out
29	Input Channel Select, Address Bit A0		
30	Input Channel Select, Address Bit A1		
31	Input Channel Select, Address Bit A2		
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"		

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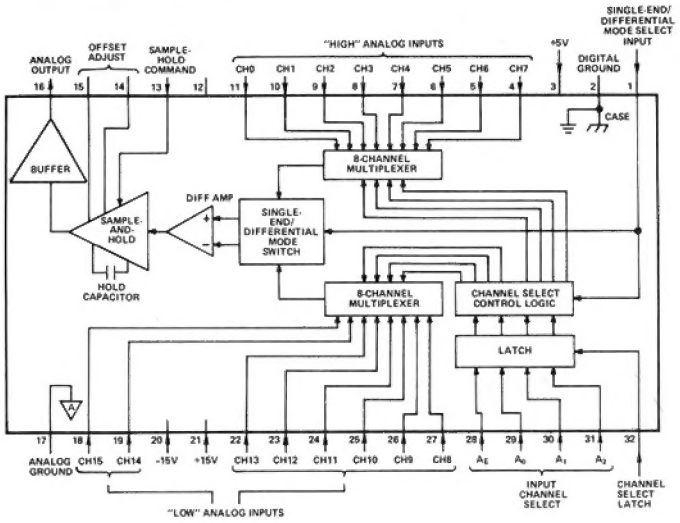

AIS Functional Block Diagram

DESIGN

Concept

Figures 1 and 2 show a general DAS application using the AD363 and AD364, respectively.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

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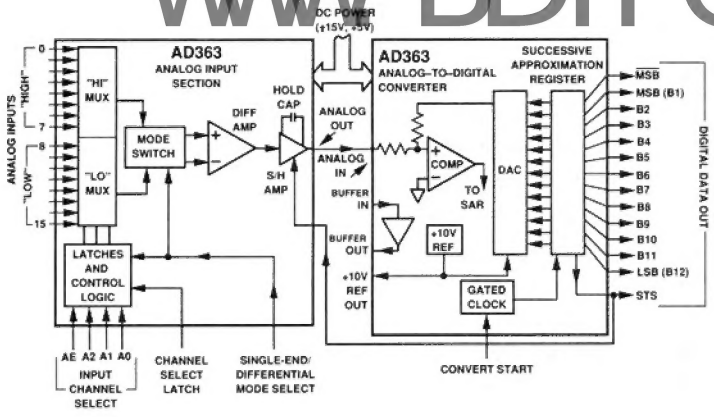

Figure 1. AD363 DAS

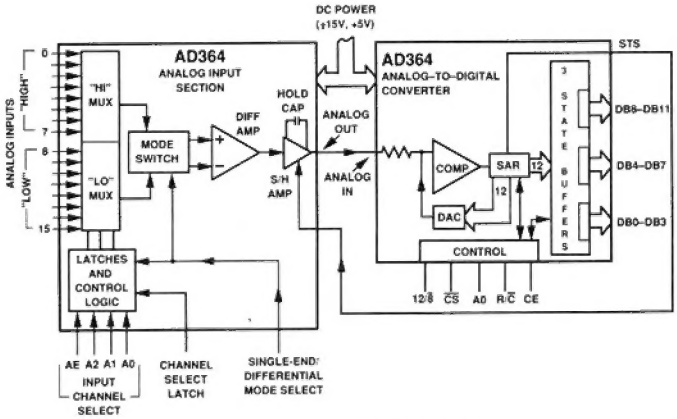

Figure 2. AD364 DAS

System Timing

Figure 3 is a general timing diagram for the circuits shown in Figures 1 and 2 operating at the maximum conversion rate.

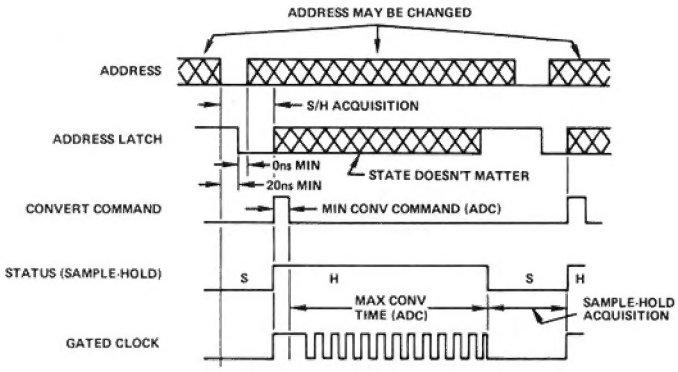

Figure 3. AD363 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy," the sample-and-hold is the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0." The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full scale (different channels may be widely varying data) the sample-and-hold will typically require 10 microseconds to"acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

AD363-ADC OPERATION

Figure 4 shows a detailed timing diagram for the AD363-ADC. Serial data changes on rising edges of the internal clock and is guaranteed to be stable on falling edges.

AD364-ADC OPERATION

There are two sets of control pins on the AD364-ADC: the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$) and the internal register controls inputs (12/$\overline{8}$ and A_O). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation, and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

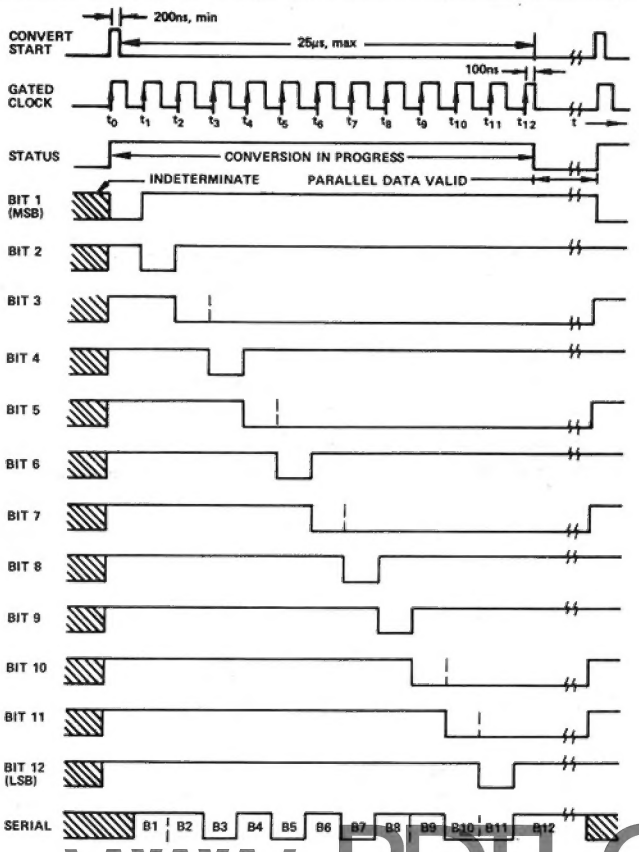

Figure 4. AD363-ADC Timing Diagram (Binary Code 110101011001)

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The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, and R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

A_O (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/$\overline{8}$ is hard-wired "high" (to V_{LOGIC}) or "low" (to Digital Common). If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_O. For these applications, the 4 LSBs (Pins 16–19) should be hard-wired to the 4 MSB (Pins 24–27). Thus, during a read, when A_O is low, the upper 8 bits are enabled and present data on Pins 20 through 27. When A_O goes high, the upper 8 data bits are disabled, the 4 LSBs then present data to Pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to Pins 20 through 23.

The A_O input performs an additional function of controlling conversion length. If A_O is held low prior to cycle initiation, a full 12-bit, 25 μs cycle will result; if A_O is held high prior to cycle initiation, a shortened 8-bit, 16 μs cycle will result. The A_O line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_O line must be properly controlled during both the convert start and read functions.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 5. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

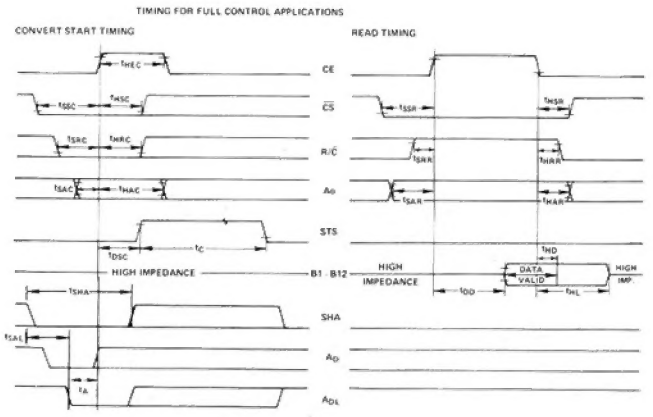

Figure 5. AD364-ADC Timing Diagram

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_O line determines the conversion cycle length and must be selected prior to conversion initiation. If A_O is low, a 12-bit cycle results; if A_O is high, an 8-bit short cycle results. Minimum setup and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held steady until STS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_O line now functions as the byte select address, with setup and hold times as shown. With A_O low, Pins 20 to 27 (DB4–11) come out of three-state and present data. With A_O high, Pins 16–19 (DB0–3) come out of three-state with data and Pins 20–23 present active trailing zeros. In the 8-bit mode, Pins 16–19 will be hard-wired directly to Pin 24–27 for direct two byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until the outputs are fully into the high impedance state.

STANDALONE OPERATION

For simpler control functions, the AD364-ADC can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_O low. There are two ways of cycling the device

TIMING SPECIFICATIONS—FULL CONTROL MODE

t_{DSC}	400 ns max	t_{DD}	200 ns max
t_{HEC}	300 ns min	t_{HD}	25 ns min
t_{SSC}	300 ns min	t_{SSR}	150 ns min
t_{HSC}	200 ns min	t_{SRR}	0 min
t_{SRC}	250 ns min	t_{SAR}	150 ns min
t_{HRC}	200 ns min	t_{HSR}	50 ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300 ns min	t_{HAR}	50 ns min
t_C	15–35 μs (12-Bit)	t_{HL}	150 ns max
	10–24 μs (8-Bit)	t_{SAL}	20 ns min
t_{SHA}	10–18 μs	t_{SA}	0 min

with this simple hookup. If a negative pulse is used to initiate conversion as in Figure 6, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 7, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low; the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

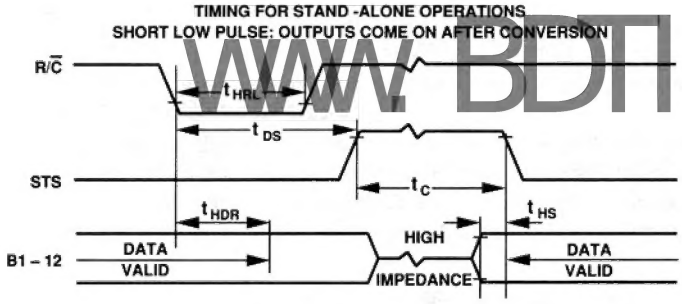

Figure 6.

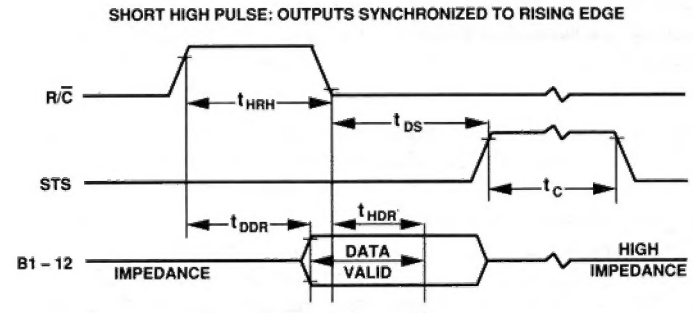

Figure 7.

TIMING SPECIFICATIONS—FULL CONTROL MODE

t_{HRL}	250 ns min	
t_{DS}	600 ns max	
t_{HDR}	25 ns max	
t_{HS}	300 ns min	1000 ns max
t_{HRH}	300 ns min	
t_{DDR}	250 ns max	

APPLICATIONS

Single-Ended/Differential Mode Control

The AIS features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to Pin 1 of the Analog Input Section:

"0": Single-Ended (16 Channels)
"1": Differential (8 Channels) (+4.0 V min)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16-single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1, and A2; AE must be enabled with a Logic "1." Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single-Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

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When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode). All unused inputs must be grounded.

Input Channel Address Latch

The AIS is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (Pin 32) is at Logic "1," input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition level-triggered.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Pin 13) is normally connected to the Status output (Pin 20) from an analog-to-digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1," putting the sample-and-hold in to the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AIS may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10 mV) relative to the AIS voltage offset and if a gain stage was to be inserted between the AIS and the ADC. To adjust the offset of the AIS, the circuit shown in Figure 8 is recommended.

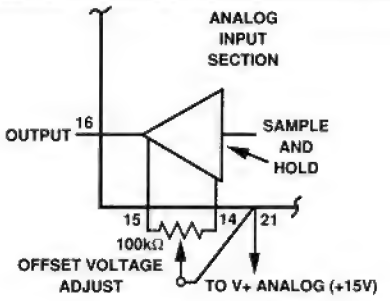

Figure 8. AIS Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Gain Adjust, AD363-ADC: Gain may be adjusted by connecting a 100 Ω potentiometer between +10 V Reference Output and Gain Adjust Input (ADC Pins 18 and 27). A multi-turn, low temperature coefficient potentiometer, such as a 20-turn cermet device, is recommended. This potentiometer may be replaced with a 50 Ω, 0.1% resistor to obtain an absolute gain calibration of 0.05% without trimming.

Offset Adjust, AD363-ADC: The simplest offset adjust circuit requires a 20-turn, 20 kΩ cermet potentiometer and a 3.9 MΩ resistor as shown in Figure 9a. This arrangement has an adjustment range of ±8 LSBs, and will contribute a maximum of 2.3 ppm/°C offset drift with a carbon composition fixed resistor (TC = −1200 ppm/°C). Drift contributions from the offset adjust circuit can be reduced well below this level using metal-film resistors and the circuit of Figure 9b.

Gain Adjust, AD364-ADC: Gain may be adjusted by connecting a 100 Ω potentiometer between the Reference Output and Reference Input (ADC Pins 8 and 10). A multi-turn, low temperature coefficient potentiometer, such as a 20T cermet device, is recommended. A fixed 50 Ω, 1% resistor should be connected between Pins 8 and 10 if no gain trim is required.

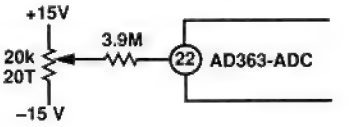

Figure 9a.

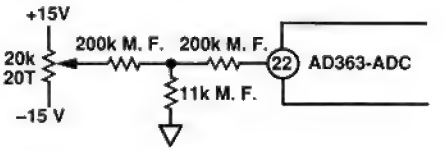

Figure 9b.

Offset Adjust, AD364-ADC: Offset adjust circuits for unipolar and bipolar operation are shown in Figures 10a and 10b. In each case the potentiometer should be a multi-turn, low temperature coefficient device, such as 20-turn cermet. Lowest offset drift in unipolar operation will be realized when the fixed resistors are low-TC (100 ppm/°C) metal-film types.

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If no offset adjustment is desired, Pin 12 should be connected to Pin 9 (unipolar mode) or to Pin 8 through a 50 Ω 1% resistor (bipolar mode).

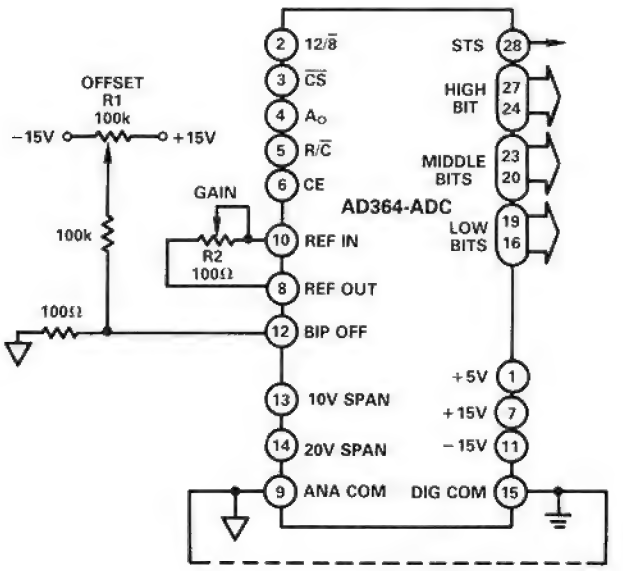

Figure 10a. Unipolar Gain & Offset

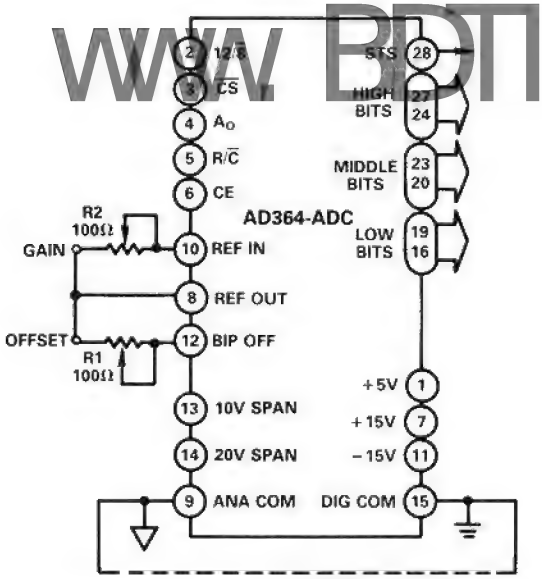

Figure 10b. Bipolar Gain & Offset

Input Scaling: Connections for the various ADC input ranges are given in Tables II and III.

Buffer: An uncommitted unity-gain buffer is available in the AD363-ADC. This buffer has a 2 μs settling time to 0.01% for a 20 V step. Its input should be grounded if the buffer is not used.

Range	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5 V	24	25 to 22	
0 to +10 V	24	—	
−2.5 V to +2.5 V	24	25 to 22	
−5 V to +5 V	24	—	22
−10 V to +10 V	25	—	

Table II. AD364-ADC Pin Connections

Range	Connect Analog Input To Pin:	Connect Pin 12 To:
0 to +10 V	13	GND*
−5 V to +5 V	13	Pin 8**
−10 V to +10 V	14	Pin 8**

*Refer to Figure 10a for gain and offset adjustments.
**Refer to Figure 10b for gain and offset adjustments.

Table III. AD364-ADC Pin Connections

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (Pin 17) and Digital Ground (Pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AIS, as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AIS they should be connected with back-to-back general purpose diodes as shown in Figure 11. This will protect the AIS from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200 mV between grounds, however this difference will be reflected directly as an input offset voltage.

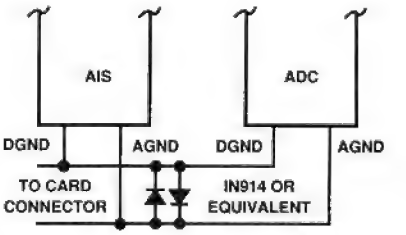

Figure 11. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15 V and +5 V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1 μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039 μF ceramic capacitor.

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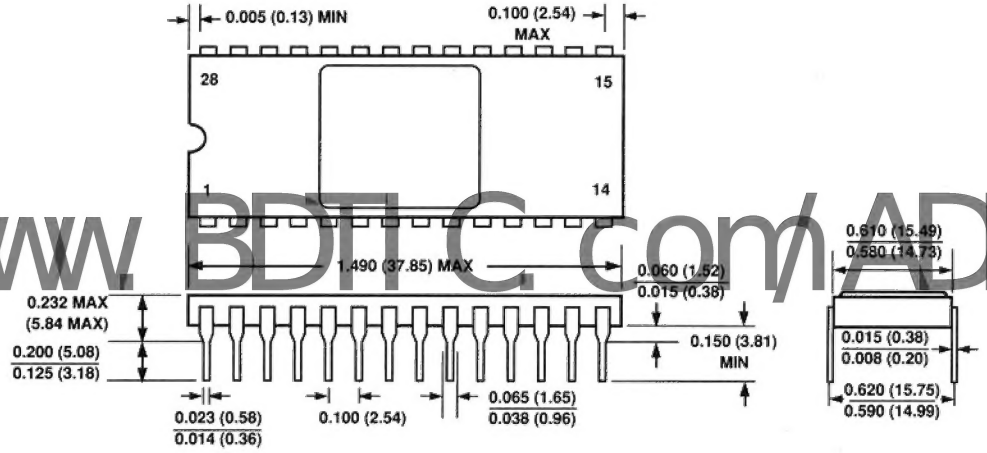
AD363/AD364 ORDERING GUIDE

Model	Temperature Range	Package Option
AD363RKD	0°C to +70°C	DH-32E (Analog Input Section) DH-32C (ADC Section)
AD363RSD	−55°C to +125°C	DH-32E (Analog Input Section) DH-32C (ADC Section)
AD364RJD	0°C to +70°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RKD	0°C to +70°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RSD	−55°C to +125°C	DH-32E (Analog Input Section) D-28 (ADC Section)
AD364RTD	−55°C to +125°C	DH-32E (Analog Input Section) D-28 (ADC Section)

D-28 Package



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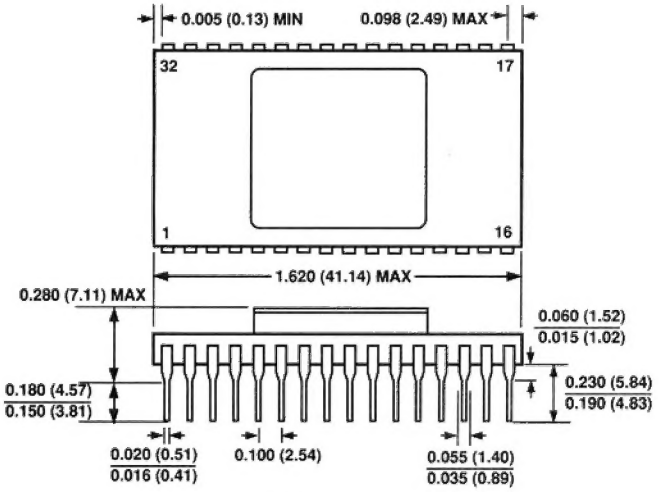
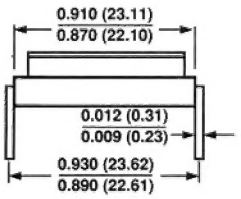
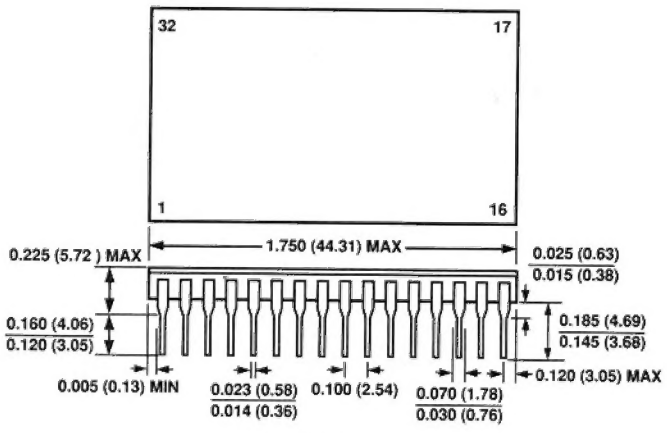
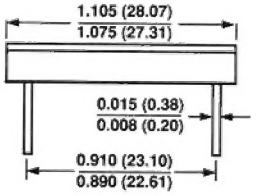
DH-32C Package





DH-32E Package





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